Abstract of the Disclosure

Disclosed are a semiconductor package device and a method for fabricating the semiconductor package device. The semiconductor package has a semiconductor chip including a plurality of bonding pads having a microscopic size and aligned at a minute interval, a planar layer formed on the semiconductor chip so as to expose the bonding pads, metal patterns formed on the planar layer and having a size larger than a size of the bonding pads in such a manner that at least some parts of the metal patterns are connected to the bonding pads and a seed metal layer interposed between the planar layer and the metal patterns. When the bonding pads have microscopic size and aligned at a minute interval, a wire-bonding process is carried out by using the metal patterns having the size larger than the size of the bonding pads and covering the bonding pad region, as a connection part to the bonding pads. Thus, the bonding pad region is reduced by 50 to 80% so that the number of chips in the semiconductor chip is increased.